In the Specification:

Please replace the paragraph starting on page 2 line 1 with the following amended paragraph:

A SIP is tested much as an individually packaged chip is tested: by being mounted on a testing board, with testing pins connected to the external connectors of the SIP. Appropriate voltages are supplied to selected external connectors, and the responses of the SIP at the same external connectors or at other external connectors are observed. The disparate nature of the various chips inside a typical SIP creates problems that do not exist in the testing of individually packaged chips. For example, a CPU typically has many external connectors to test, but the time of the test **[[if]]** is relatively short (several seconds). By contrast, a memory chip typically has a small number of external connectors to test, but the test may take upwards of ten minutes because each bit of the memory chip must be tested by writing to the bit and then reading the bit. In the case of individually packaged chips, relatively few CPUs can be tested simultaneously, but the test time is relatively short. Conversely, many individually packaged memory chips can be tested together, but the test time is relatively long. Nevertheless, the overall throughputs of individually packaged CPUs and individually packaged memory chips under test are similar. Testing a SIP that includes a CPU and one or more memory chips gets the worst of both worlds: the duration of the test is long, to accommodate the memories; but many testing pins must be provided to access for testing, not only the CPU and the memories, but also the internal connections that constitute the internal interface between the CPU and the memories.